1. (a) Tabulate the comparison between CMOS and Bipolar technologies.
   (b) Explain the concepts of ‘Lithography’ and ‘Probe testing’ related to IC production process. [8+8]

2. (a) Deduce the expressions for drain-to-source current versus drain-to-source voltage relations.
   (b) Find the pull-up to pull-down ratio for an nMOS inverter driven through one or more pass transistors. [8+8]

3. (a) Explain with suitable diagrams, the lambda-based design rules.
   (b) Draw the symbolic layout for the CMOS inverter and give the general CMOS logic-gate layout guidelines. [8+8]

4. (a) Draw and explain fan-in and fan-out characteristics of different CMOS design technologies.
   (b) Explain in detail about formal estimation of CMOS Inverter delay. [8+8]

5. (a) Describe the nature of a parity generator and explain its structured design approach.
   (b) Draw a four-bit Braun multiplier and give its subsystem level design considerations. [8+8]

6. (a) Draw the general architecture of programmable logic array and explain.
   (b) Explain the design flow of standard cell with neat diagram. [8+8]

7. (a) Explain the following with respect to VHDL synthesis.
    (i) Simulation  (ii) layout
   (b) Describe VHDL synthesis approach with an example. [8+8]

8. (a) What is meant by CMOS testing? Explain the need for testing.
   (b) Discuss about layout design for improved testability. Consider a suitable example. [8+8]
Code No: V3219/R07

III B.Tech II Semester Regular & Supplementary Examinations, April/May - 2012

VLSI DESIGN
(Common to Electrical and Electronics Engineering & Electronics and Communication Engineering & Biomedical Engineering)

Time: 3 Hours Max Marks: 80

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Give the comparison between CMOS and Bipolar technologies.
    (b) Explain the IC production process concept of ‘Oxidation’ and ‘Ion Implantation’.

2. (a) Draw and explain the characteristics of nMOS transistor in different modes of operation and its body effect.
    (b) Explain the design considerations of Bi-CMOS inverter with suitable circuit diagram

    (b) What are limitations of scaling for VLSI circuits and briefly explain them.

4. (a) Discuss about area capacitances of MOS layers and give area capacitance calculations with suitable examples.
    (b) Explain the concepts of ‘nMOS inverter pair delay’ and ‘Minimum size CMOS inverter pair delay’ with necessary circuit diagrams.

5. (a) Elaborate the concept of pipelining relevant to subsystem design principles.
    (b) Explain step-by-step subsystem design approach. Consider adder as an example.

6. (a) Explain semiconductor integrated circuit design approach using programmable logic arrays.
    (b) Write notes on Complex Programmable Logic Devices.

7. (a) Explain the VLSI circuit design flow with neat flow diagram.
    (b) What are the various VHDL verification tools? Explain any one of item.

8. (a) Describe the various design strategies used for CMOS testing.
    (b) What are the system-level test techniques? Explain one of them with an example.

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1. (a) Explain step-by-step procedure for a typical n-well process with neat diagrams.
   (b) Describe the terms ‘Metallization’ and ‘Encapsulation’ relevant to IC fabrication process.

2. (a) Define the following with necessary expressions.
   (i) $g_m$
   (ii) $g_{ds}$
   (iii) Figure of Merit
   (b) Write notes on MOS transistor threshold voltage.

3. (a) Tabulate the encoding scheme for a simple single metal nMOS process with respect to various MOS layers.
   (b) Define and give the expressions for any four scaling factors of MOS device parameters.

4. (a) What is meant by sheet resistance $R_s$? Explain the concept of $R_s$ applied to MOS transistors.
   (b) What are the alternate gate circuits are available? Explain any one of item with suitable sketch.

5. (a) What are Wallace tree elements? Give and explain an example of the Wallace tree approach.
   (b) Draw and give the design approach for a carry look ahead adder with its structure.

6. (a) Illustrate how logic functions can be realized using nMOS PLA with an example.
   (b) Discuss about Field Programmable Gate Arrays.

7. (a) Draw the block diagram of synthesis process and illustrate with an example.
   (b) List the various VHDL verification tools and explain any one of them.

8. (a) Describe the design strategies for CMOS testing.
   (b) Explain the concept of layout design for improved testability with suitable example.
VLSI DESIGN
(Common to Electrical and Electronics Engineering & Electronics and Communication Engineering & Biomedical Engineering)

Time: 3 Hours  Max Marks: 80

Answer any FIVE Questions
All Questions carry equal marks

1. (a) Explain the nMOS fabrication process with suitable diagrams
   (b) Explain the processing steps used in IC fabrication process.  [8+8]

2. (a) Draw and explain their significance of various pull up forms.
   (b) Give the design aspects and draw the circuit diagram of nMOS inverter and with the help of transfer characteristics.  [8+8]

3. (a) Explain the ‘VLSI Design Flow’ with neat flow diagram.
   (b) Present the general CMOS logic-gate layout guidelines and draw the user defined layout drawing conventions.  [8+8]

4. (a) What is meant by standard unit of capacitance? Give some area capacitance calculations.
   (b) Illustrate driving large capacitive loads with relevant examples.  [8+8]

5. (a) Give the subsystem design considerations of a four-bit adder.
   (b) Draw and explain the architecture of a high-density memory system.  [8+8]

6. (a) Differentiate PAL and PLA with respect to various performance parameters.
   (b) Compare the performance parameters of Complex Programmable Logic Devices and Field Programmable Gate Arrays.  [8+8]

7. (a) Explain any one of the design capture tools available for VHDL synthesis with an example.
   (b) With suitable block diagrams, explain the terms ‘Hardware Simulation’ and ‘Synthesis Process’.  [8+8]

8. (a) Explain the CMOS testing principles.
   (b) Write notes on system-level CMOS testing techniques.  [8+8]